Dr. Jitendra Kanungo

Associate Professor

Education: M. Tech., Ph.D. (IIT Roorkee)

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Areas of Interest: Ultra low power digital circuit design, circuit/device co-design issues.

Brief Profile:

Dr. Jitendra Kanungo has completed Ph.D. in the area of Ultra Low Power VLSI Circuit Design from Department of Electronics & Communication Engineering, Indian Institute of Technology (IIT) Roorkee in year 2013. He has received M. Tech. (Micro-electronics) degree from University Centre for Instrumentation & Microelectronics (UCIM), Panjab University Chandigarh in year 2003 and M.Sc. (Electronics) degree from School of Electronics (SOE), Devi Ahilya University Indore in year 2001. During August 2004 to July 2007, he was Lecturer (ECE) in the College of Engineering Roorkee (COER). During July 2007 to July 2008, he has worked as Research Fellow in the project SMDP-II at the Department of Electronics & Computer Engineering, IIT Roorkee. This project was governed by the Ministry of Communication & Information Technology (MCIT), Govt. of India. He has published more than 40 research papers in peer reviewed journals and international conferences.

Membership: Senior Member-IEEE

Ph. D. Supervision

Research Scholar Status

1. Mr. Durgesh Nandan : Awarded
2. Mr. Dharmendra Jain : Awarded
3. Mr. Beerendra Kumar Patel : Awarded

M. Tech. Supervision

1. Trapti Mudgal (2016)
2. Mr. Beerendra Kumar Patel (2015)

Reviewer of International Journals:

1. IEEE Access
2. IET, Circuits, Devices and Systems
3. Springer Journal of Circuits, Systems and Signal.
4. Journal of Institution of Engineers (India)- Series B
5. JUET Research Journal of Science & Technology
6. Journal of Microelectronics and Solid State Electronics, Scientific & Academic Publishing (SAP), USA.

Publication@JUET

Publication Details Google Scholar Profile

Journal

1. Durgesh Nandan, Jitendra Kanungo, and Anurag Mahajan, "An error-efficient Gaussian filter for image processing by using expanded operand decomposition logarithm multiplication," Springer, Journal of ambient intelligence and humanized computing, vol. 15, pp. 1045-1052, January 2024.

2. Dharmendra Jain, S. K. Tripathi, Jitendra Kanungo, and B. L. Gupta (2023), "Fabrication and characterization of supercapacitor comprising mango kernel derived electrode under different electrolyte system," Wiley Journal of Energy Storage, vol. 5, no. 3, pp. 1-10, March 2023. DOI: https://doi.org/10.1002/est2.465

3. Beerendra Kumar Patel and Jitendra Kanungo, "Design of an Efficient Reverse Converter for Moduli Sets 24p+1, 2p+1, 2p-1, 22p+1, 22p", Journal of Engineering Research, ICMET Special Issue, pp. 1-16, 2022.

4. Beerendra Kumar Patel and Jitendra Kanungo, "Area efficient Diminished-1 Modulo 2n-1 1 Adder using Parallel Prefix Adder", Journal of Engineering Research, pp. 8-18, 2022.

5. Durgesh Nandan, Anurag Mahajan, and Jitendra Kanungo, "An Efficient VLSI Architecture Design of Antilogarithm Converter with 10-Regions Error Correction Scheme", Mathematical Modelling of Engineering Problems vol. 8, no. 2, pp. 213-218, 2021.

6. Dharmendra Jain, Jitendra Kanungo, and S. K. Tripathi, "Enhancement in performance of supercapacitor using eucalyptus leaves derived activated carbon electrode with CH3COONa and HQ electrolytes: step towards environment benign supercapacitor", Journal of Alloys and Compounds vol. 832, article no. 154956, 2020.

7. D. Jain, J. Kanungo, and S. K. Tripathi, "Performance enhancement approach for supercapacitor by using mango kernels derived activated carbon electrode with p-hydroxyaniline based redox additive electrolyte", Elsevier journal of Materials Chemistry and Physics, vol. 229, pp. 66-77, May, 2019.

8. Dharmendra Jain, Jitendra Kanungo, and SK Tripathi, "Synergistic effect of redox couple VO2+/VO2+ with H3PO4 to enhance the supercapacitor performance," Springer Journal of Materials Science: Materials in Electronics, Vol. 30, no. 13, pp. 12244-12259, May 2019.

9. Dharmendra Jain, Jitendra Kanungo, and S. K. Tripathi, "Synergistic Approach with Redox Additive for the Development of Environment Benign Hybrid Supercapacitor", Journal of The Electrochemical Society vol. 166(14), pp. A3168-A3181, 2019.

10. Durgesh Nandan, Kanungo, J. and Mahajan, A. (2018), "An errorless Gaussian filter for image processing by using expanded operand decomposition logarithm multiplication," Springer, Journal of ambient intelligence and humanized computing, July 2018.

11. Dharmendra Jain, Jitendra Kanungo and S. K. Tripathi, “Enhanced performance of ultra-capacitors using redox additive based electrolytes”, Applied Physics A, vol. 124, pp.397, May 2018.

12. Durgesh Nandan, Mahajan A. and Jitendra Kanungo, “An efficient VLSI architecture design of Leading One Detector,” International journal of pure and applied mathematics, vol. 118, no. 14, pp. 267-272, 2018.

13. Durgesh Nandan, Kanungo, J. and Mahajan A., “An efficient architecture of Iterative Logarithmic Multiplier,” International journal of engineering & technology (UAE), vol. 7, no. 2.16, pp. 24-28, 2018.

14. Durgesh Nandan, Kanungo, J. and Mahajan A., “65 years journey of logarithm multiplier,” International journal of pure and applied mathematics, vol. 118, no. 14, pp. 261-266, 2018.

15. Beerendra Kumar Patel, and Jitendra Kanungo, “Diminished-1 multiplier using modulo adder”, International Journal of Engineering & Technology”, vol. 7, no. 4.20, pp.31-35, 2018.

16. Durgesh Nandan, Jitendra Kanungo and Anurag Mahajan “An Efficient VLSI architecture design for logarithmic multiplication by using the improved operand decomposition,” Elsevier, VLSI the integration journal, Vol. 58, pp. 134-141, June 2017.

17. Durgesh Nandan, Jitendra Kanungo and Mahajan A., “Implementation of Leading One Detector based on reversible logic for logarithmic arithmetic,” International Journal of Computer Applications, vol. 173, no. 8, pp. 40-45, Sep. 2017.

18. Hemant Sharma, Samyak Tomar and Jitendra Kanungo, “FPGA Implementation of 4-Bit Parallel Cyclic Redundancy Code,” International Journal of Research in Engineering and Technology, vol. 4, no. 11, pp. 111-113, Nov. 2015.

19. Jitendra Kanungo and S. Dasgupta, ” Analysis of Energy-Efficient Single Phase Adiabatic Logic at Sub-100 nm CMOS Technology,” JUET Research Journal of Science & Technology, vol. 2, no. 1, pp. 133- 138, Jan. 2015.

20. Jitendra Kanungo and S. Dasgupta, “Sinusoidal Clocked Sense-Amplifier Based Energy Recovery Flip-Flops,” World Scientific Journal of Circuits, Systems and Computers, vol. 23, no. 5, pp. 1450066-1-1450066-19, March 2014.

21. Jitendra Kanungo and S. Dasgupta, ”Performance Analysis of a Complete Adiabatic System Driven by the Proposed Power Clock Generator” IOP Science, Journal of Semiconductors, vol. 35, no. 9, pp. 095001-1- 095001-7, Sep. 2014.

22. Jitendra Kanungo and S. Dasgupta, “An Efficient Single Phase Adiabatic Logic and its Application to Combinational and Sequential Design”, ASP Journal of Low Power Electronics, vol. 7, no. 3, pp.381-393, Aug. 2011.

23. Jitendra Kanungo and S. Dasgupta, “Energy Estimation for an n-input Adiabatic Logic Gate: A Proposed Analytical Model,” World Scientific Journal of Circuits, Systems and Computers, vol. 22, no. 5, pp. 1350037-1-1350037-19, Apr. 2013.

24. Jitendra Kanungo and S. Dasgupta, “Single Phase Energy Recovery Logic and Conventional CMOS Logic: A Comparative Analysis,” Journal of Microelectronics and Solid State Electronics, Scientific & Academic Publishing (SAP), USA, vol. 2, no. 2A, pp. 16-21, Apr. 2013.

25. Jitendra Kanungo and S. Dasgupta,”Study of Scaling Trends in Energy Recovery Logic: An Analytical Approach,” IOP Science, Journal of Semiconductors, vol. 34, no. 8, pp. 085001-1-085001-5, Aug. 2013.

Conference

1. Beerendra Kumar Patel and Jitendra Kanungo (2021), “Efficient tree multiplier design by using modulo adder,” Proc. IEEE Emerging Trends in Industry 4.0 (ETI 4.0), pp.1-6. DOI:10.1109/ETI4.051663.2021.9619220.

2. Dharmendra Jain, Jitendra Kanungo, and S. K. Tripathi, “Characterization of Supercapacitor for the Development of Energy Storage Units”, International Conference on Signal Processing and Communication (ICSC- 2019) organized at JIIT, Noida, pp. 264-270, during March 07-09, 2019.

3. Durgesh Nandan, Kaushal Kumar, Jitendra Kanungo, Ritesh Kumar Mishra (2018), “Compact and errorless 16-region error correction scheme for antilogarithm converter”, Proc. International Conference on Electrical, Electronics and Computer Engineering (UPCON), pp.1-5.

4. Durgesh Nandan, Jitendra Kanungo and Anurag Mahajan, “An efficient VLSI architecture for Iterative Logarithmic Multiplier,” IEEE 4th International conference on Signal Processing and Integrated Networks (SPIN), Noida, pp.419-423, Feb.2017.

5. Durgesh Nandan, Mahajan, A. and Jitendra Kanungo, “An Efficient antilogarithmic converter by using 11-regions error correction scheme,” IEEE 4th International Conference on Signal Processing, Computing and Control (ISPCC 2017), JUIT, Waknaghat, 21-23 Sep.2017, pp. 118-121.

6. Durgesh Nandan, Jitendra Kanungo and Anurag Mahajan, “An efficient antilogarithmic converter by using 11-regions error correction scheme,” 4th IEEE International Conference on Signal Processing, Computing and Control (ISPCC 2k17), Sep. 21-23, 2017, Solan, India.

7. Durgesh Nandan, Jitendra Kanungo and Anurag Mahajan, “An Efficient VLSI architecture design for antilogarithmic converter by using the error correction scheme,” IETE International conference on signal processing (ICSP), SATI, Vidisha, 11-13 Nov. 2016.

8. Jitendra Kanungo, and S. Dasgupta, “The Study of Energy Efficiency of Single Phase Energy Recovery Logic with Progressive Technology," Symposium on VLSI Design and Testing 2011 (VDAT-2011), Pune, pp. 1-10, July 7-9, 2011.

9. Jitendra Kanungo, and S. Dasgupta, “Key Challenges in Adiabatic Logic Circuits at sub-100 nm Scale,” International conference on communication, computers and devices (ICCCD), IIT Kharagpur, pp. 1-4, Dec. 10-12, 2010.

10. Jitendra Kanungo, and S. Dasgupta, “Performance Analysis of 4 x 4 Array Multiplier Units using various Full Adder Cells at 70 nm Scale,” 15th International Workshop on The Physics of Semiconductor Devices (IWPSD), Delhi (India), December 15-19, 2009.
Patent Published: Indian Design Patent “Object/Motion Detection Based Public Lighting Fixture”, Jan. 2023.