NATIONAL WORKSHOP On

High-performance VLSI Architectures for Digital Signal Processing Applications: Design and Implementations

September 9-11, 2016

Registration Form

Name: _____

Designation: _____

Qualification: _____

Organization: _____

E-mail:_____

Phone:_____

Demand Draft* no.: _____

Dated_____ Amount Rs._____

Draw on_____

Signature of participant

* Draft should be drawn in favor of "Jaypee University of Engineering and Technology", payable at Guna.

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Dr. Jitendra Kanungo, Mr. Subodh K. Singhal
Mr. Sujit K. Patel

Program Chair
Dr. B.K.Mohanty
Professor and Head, ECE

Coordinator
Dr. Anurag Mahajan
Assistant Professor (SG), ECE
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Who can participate?
Faculty members**,** research scholar and PG students working on VLSI and signal processing

Registration
Registration is compulsory for participation. A limited number of seats are available. Registration will be confirmed on first cum first served basis.

Registration fee: Rs. 500/ (include workshop participation for 3 days)

On campus accommodation is available on payment basis: Rs. 500/ per day (include breakfast, lunch, and dinner)
Completed registration form along with DD of the desired amount should reach to the Workshop Coordinator by **September 2, 2016**.

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Organized by

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Electronics & Communication Engineering
Jaypee University of Engineering & Technology
AB-Road, Raghogarh, Guna,
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Sponsored by: M.P. Council of Science &Technology, Bhopal

About JUET

Jaypee University of Engineering and Technology was established in the year 2003 in the name of Jaypee Institute of Engineering & Technology based on the MOU signed between Jaiprakash Sewa Sansthan and the Government of Madhya Pradesh with an aim of becoming a Center of Excellence in Engineering and Technology. The Government of MP has (vide gazette extra ordinary no. 3 of 2010) established Jaypee University of Engineering and Technology (JUET), Raghogarh, Guna as the first private university in the State of MP under the provisions of MP Niji Vishwavidyalaya Adhiniyam 2007. It has been approved by UGC under section 2(f) of UGC Act, 1956. The Electronics & Communication Engineering Department was established in 2003, and offers B. Tech, M.Tech and Ph.D. programmes.

About Workshop

Digital signal processing (DSP) is a ubiquitous technology which plays the central role in many different areas of applications, e.g., audio, video, image and speech processing, communications, healthcare, automotive safety and surveillance, safety and security of underground pipelines transporting water, oil and natural gas, and many more. Typical DSP algorithms are computation-intensive, and its application demand real-time processing. Application specific computing architectures are necessary to meet the performance specification. The objective of this workshop is to provide theoretical background and hands on training to the participants on design and implementation aspects of DSP algorithms in ASIC and FPGA for resource constrained applications. Subject experts will take part in this workshop to deliver lectures and conduct hands-on practice sessions.

Topics to be covered in lecture session

- Typical DSP algorithms and complexity analysis
- Algorithm mapping and architectural design Arithmetic circuit design
- Low-power/low-complexity design techniques
- ASIC and FPGA implementation

Topics for hands-on practice:

- HDL coding circuit synthesis using Xilinx ISE tools.
- Implementation of DSP algorithm in FPGA board
- ASIC Synthesis using Synopsys Design Compiler

Resource Persons

Mohammad Hasan (Electronics Engg. Dept., AMU)
Prof. Hasan completed his PhD from the University of Edinburgh, UK on a Commonwealth Scholarship in "Low Power Architectures for Signal Processing and Communications". He also worked as a Visiting Researcher in Royal Academy of Engineering, UK funded project on "Low Power FPGA".

Basant Kumar Mohanty (ECE Dept., JUET)
Prof. Mohanty received his Ph.D degree in VLSI for Digital Signal Processing. His research interest includes algorithm design, mapping and implementation for high-performance, resource-constrained multi-media signal processing applications and secured communication.

Samrat Sabat (University of Hyderabad)
Prof. Samrat Sabat received Ph.D. in Electronic Sciences from Berhampur University in 2004 currently working as an Associate Professor at Center for Advanced studies in Electronics Science and Technology in the School of Physics, His research interest includes development of signal processing algorithms for cognitive radio, smart sensors and implementation in FPGA and System on Chip.

Subhendu Kumar Sahoo (BITS,Pilani Hyderabad campus)
Dr. S. K. Sahoo received Ph.D. from BITS Pilani and currently working as Associate Professor in EEE department of BITS Pilani, Hyderabad campus. His research interest includes development of signal processing algorithms and architectures for DSP applications.

Anurag Mahajan (ECE Dept., JUET)
Dr. Anurag Mahajan received Ph.D. from JUET, Guna and working as Assistant Professor (SG) in ECE department at JUET, Guna. His research interest includes VLSI architectures for DSP applications.

Jitendra Kanungo (ECE Dept., JUET)
Dr. Jitendra Kanungo received Ph.D. from IIT, Roorkee and working as Assistant Professor (SG) in ECE department at JUET, Guna. His research interest includes Ultra low power VLSI circuit design.

Subodh K. Singhal (ECE Dept., JUET)
Mr. Subodh K. Singhal currently pursuing Ph.D. from JUET, Guna and working as Assistant Professor (G-II) in ECE department at JUET, Guna. His area of interest is VLSI Design.

Sujit K. Patel (ECE Dept., JUET)
Mr. Sujit K. Patel currently pursuing Ph.D. from JUET, Guna and working as Assistant Professor (G-II) in ECE department at JUET, Guna. His area of interest is VLSI Design,
back end Tools.

Tentative Schedule

Day 1: 9 September 2016	
Time	**Event**
9.00 am - 9.30 am	Registration
9.30 am - 10.00 am	Inaugural session
10.00 am -10.30 am	Tea break
10.30 am - 12.30 pm	**Talk 1**: VLSI architectures for DSP algorithms (**Prof. Mohammad Hasan**)
12.30 pm - 1.30 pm	**Lunch Break**
1.30 pm - 3.30 pm	**Talk 2**: Low power VLSI design (**Prof. Mohammad Hasan**)
3.30 pm - 3.45 pm	**Tea Break**
3.45 pm - 5.45 pm	**Lab session 1**: HDL coding and synthesis using ISE tools (**Dr. A. Mahajan & Mr. S. K Patel**)
Day 2: 10 September 2016	
Time	**Event**
9.15 am - 11.15 am	**Talk 3**: Computational complexity analysis of typical DSP algorithms and design strategies (**Prof. B.K.Mohanty**)
11.15 am - 11.30 am	**Tea Break**
11.30 am - 1.30 pm	**Talk 4**: Design and implementation of DSP algorithm on FPGA (**Dr. Samrat Sabat**)
1.30 pm - 2.30 pm	**Lunch Break**
2.30 pm - 3.30 pm	**Lab session 2**: FPGA design flow using Vertex-6 board (**Dr. Samrat Sabat and Mr.S.Singhal**)
3.30 pm - 3.45 pm	**Tea Break**
3.45 pm - 5.45 pm	**Lab session 2**: FPGA design flow using Vertex-6 board (**Dr. Samrat Sabat and Mr.S.Singhal**)
Day 3: 11 September 2016	
Time	**Event**
9.15 am - 11.15 am	**Talk 5**: Low-complexity design using distributed arithmetic (**Prof. B.K.Mohanty**)
11.15 am - 11.30 am	**Tea Break**
11.30 am - 1.30 pm	**Talk 6**: Recent trend on multiplier design (**Dr.S.K.Sahoo**)
1.30 pm - 2.30 pm	**Lunch Break**
2.30 pm - 4.30 pm	**Lab session 3**: HDL coding of arithmetic circuits and synthesis using Synopsys Design Compiler (**Dr.S.K.Sahoo & Dr. J.Kanungo**)
4.30 pm - 5.15 pm	Valedictory Session
5.15 pm - 5.30 pm	High Tea